PHASE LOCK LOOP APPLYING IN WIRELESS COMMUNICATION SYSTEM AND METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the invention

This present invention relates to a phase lock loop, and more particularly, the present invention relates to a phase lock loop applied in wireless communication systems.

2. Description of the prior art

In a wireless communication system, a phase lock loop is used to generate a transmission signal that has specific phase and specific frequency. In a conventional phase lock loop, the specific frequency is generated through the following steps: first, generating a local oscillating frequency by a frequency synthesizer; next, dividing the local oscillating frequency by a fixed divider and inputting the signal with a reduced frequency into the phase detector; then, generating a control signal; and finally, generating the specific frequency by the control signal. Therefore, for the same specific frequency, the corresponding local oscillating frequency is fixed. However, because of the noise interference, the signal quality of the corresponding fixed local oscillating frequency becomes worse, and the signal quality of the transmission signal of the phase lock loop is also worsened.

There are several kinds of frequency synthesizer, but each of them has different kinds of noise interferences. For example, the interference caused by the multiplied frequency of the crystal oscillator frequency, that is when the desired local oscillating frequency approaches the multiples of a certain spur frequency, the local oscillating

frequency is easily interfered. Thus, around the desired local oscillating frequency from several kHz to 1MHz, there will be some interference signals.

The conventional method for preventing the noise interference focused on the improvement of the frequency synthesizer, but that will make the circuit more complicated and increase the cost of production. When the problem of interference remains unsolved, that frequency might not be usable, or that frequency might have a lower usage quality.

SUMMARY OF THE INVENTION

An objective of the invention is to provide a phase lock loop that applies in wireless communication systems and a method for generating a RF signal. The phase lock loop is used to receive a baseband signal that has an input frequency and modulate the baseband signal to be a corresponding RF signal. The RF signal has a predetermined transmission frequency for transmitting.

According to a preferred embodiment of the present invention, the phase lock loop comprises a frequency synthesizer, a first programmable divider, a modulator, a voltage-controlled oscillator, and a frequency converter. The frequency synthesizer is used to generate a local oscillating signal that has a local oscillating frequency. The first programmable divider is used to divide the frequency of the local oscillating signal by a first programmable divisor to generate a reference signal. The modulator is used to modulate the frequency of the reference signal according to the baseband signal to generate a corresponding first comparison signal. The voltage-controlled oscillator (VCO) is used to generate the corresponding RF signal for transmitting according to the corresponding control voltage generated by the phase difference between the first comparison signal and a second comparison signal. The RF signal is fed back as a feedback signal. The frequency converter is used to receive the feedback signal and the local oscillating signal and output the second comparison signal to the phase detector in responsive to the frequency difference of the feedback

signal and the local oscillating signal. The first programmable divisor of the first programmable divider is programmable-controlled so as to prevent the occurrence of a spur frequency in the RF signal, besides the predetermined transmission frequency, due to the interfered local oscillating signal.

According to the phase lock loop of the present invention, the first programmable divisor of the first programmable divider is programmable-controlled so as to prevent the occurrence of a spur frequency in the RF signal, besides the predetermined transmission frequency, due to the interfered local oscillating signal. By using the present invention, all channels of the global system for mobile communication (GSM) can select a suitable local oscillating frequency, without having problems of low quality output signals.

The advantage and spirit of the invention may be understood by the following recitations together with the appended drawings.

BRIEF DESCRIPTION OF THE APPENDED DRAWINGS

FIG. 1 is a function block diagram of a phase lock loop according to the present invention.

FIG. 2 is a function block diagram of a phase lock loop according to another preferred embodiment of the present invention.

FIG. 3 is an experimental data curve of the transmission frequency as the first programmable divisor M of the phase lock loop 30, shown in FIG. 2, is equal to 11.

FIG. 4 is an experimental data curve of the transmission frequency as the first programmable divisor M of the phase lock loop 30, shown in FIG 2, is equal to 9.

FIG. 5 is an experimental data curve of the transmission frequency modulated by the baseband signal shown in FIG. 3.

FIG. 6 is an experimental data curve of the transmission frequency modulated by the baseband signal shown in FIG. 4.

FIG. 7 is a flow chart of the generating method of the RF signal of the phase lock loop shown in FIG. 2.

FIG. 8 is a function block diagram of a phase lock loop according to another preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a phase lock loop, which applies in the RF signal transmission device of a wireless communication system, for receiving a baseband signal that has an input frequency (F_i) and modulating the baseband signal to be a corresponding RF signal (F_{tx}); the RF signal has a predetermined transmission frequency for transmitting.

Referring to FIG. 1, FIG. 1 is a function block diagram of a phase lock loop 10 according to the present invention. The phase lock loop 10 comprises a frequency synthesizer 12, a first programmable divider 14, a modulator 16, a phase detector 18, a charging pump 20, a loop filter 22, a voltage-controlled oscillator 24, and a frequency converter 26.

The frequency synthesizer 12 is used to generate a local oscillating signal that has a local oscillating frequency F_{LO}. The first programmable divider 14 divides the frequency of the local oscillating signal by a first programmable divisor M to generate a reference signal S_{re}. The modulator 16 modulates the frequency of the reference signal S_{re} according to the baseband signal to generate a corresponding first comparison signal S_1.

The phase detector 18 is used to detect phases of the first comparison signal S_1 and a second comparison signal S_2 and output a corresponding current-controlled I/O

signal S_{IQ} in response to the phase difference between the two comparison signals. The charging pump 20 is used to receive the current-controlled I/O signal S_{IQ} and accordingly output a corresponding control current I. The loop filter 22 filters the control current I to output a control voltage V to the voltage-controlled oscillator 24.

The voltage-controlled oscillator 24 generates the corresponding RF signal for transmitting, according to the control voltage V. The RF signal is fed back as a feedback signal S_{FB}. The frequency converter 26 receives the feedback signal S_{FB} and the local oscillating signal to output the second comparison signal S_2 to the phase detector 18 in response to the frequency difference between the feedback signal S_{FB} and the local oscillating signal.

The first programmable divisor M of the first programmable divider 14 is programmable-controlled so as to prevent the occurrence of a spur frequency, besides the predetermined transmission frequency, in the RF signal due to the interfered local oscillating signal.

The following paragraphs describe how to prevent the local oscillating signal from being interfered by the first programmable divisor M that is programmable-controlled.

When the transmission frequency of the RF signal of the phase lock loop 10 is F_{tx}, the relative equation between F_{LO} and the first programmable divisor M is $F_{LO} = \frac{(M-1)}{M} \times F_{tx}$. F_{tx} is a fixed value, and the conventional first programmable divisor M is also a fixed value. If the present result F_{LO} is interfered by the other signal, the conventional method of changing the circuit can not solve the interference problem effectively. Therefore, if the first programmable divisor M is programmable-controlled, another F_{LO} can be calculated to complete the phase lock loop 10 and obtain the same F_{tx}.

For example, the global system for mobile communication(GSM) uses the channel 631 as the signal transmission channel. The frequency of this channel is

1734MHz. If the programmable divisor N is fixed as 9, from the equation $F_{LO} = \frac{(M-1)}{M} \times F_{tx}$, F_{LO} can be calculated as 1950.75MHz. However, the frequency 1950.75MHz is very easily interfered by the multiple frequency of the reference frequency 13MHz or 26MHz that are often used by the frequency synthesizer of the global sim mobile system. In this situation, the first programmable divisor is changed to 11, and then F_{LO} becomes 1907.41MHz. The frequency 1907.4MHz is 43.35MHz apart from the frequency 1950.65MHz, and the frequency 1907.4MHz can prevent the interference from the multiple frequency of the reference frequency 13MHz or 26MHz.

Referring to FIG. 2, FIG. 2 is a function block diagram of a phase lock loop 30 according to another preferred embodiment of the present invention. Comparing the phase lock loop 10 in FIG. 1 with the phase lock loop 30 in FIG. 2, the phase lock loop 30 further comprises a phase shift generator 32 and a second programmable divider 34. The phase shift generator 32 is used to shift the phase of the reference signal S_{re} generated by the first programmable divider 14 by 90 degrees, and then input the phase-shifted reference signal into the modulator 16. Before the local oscillating signal enters the frequency converter 26, the frequency of the local oscillating signal is first divided by the second programmable divisor N in the second programmable divider 34, and then the frequency-divided local oscillating signal enters the frequency converter 26.

In the phase lock loop 30, the transmission frequency F_{tx} of the RF signal, the local oscillating frequency F_{LO} of the local oscillating signal, the first programmable divisor M of the first programmable divider 14, and the second programmable divisor N of the second programmable divider 34 satisfy the following equation:

$$F_{tx} = \left(\frac{M \pm N}{M \times N}\right) \times F_{LO}$$

By this method, for the transmission frequency F_{tx} of the fixed RF signal of the

phase lock loop, the better local oscillating frequency F_{LO} can be selected by changing the first programmable divisor M of the first programmable divider 14 and the second programmable divisor N of the second programmable divider 34, so as to avoid interfering the output signal of the phase lock loop by the specific local oscillating frequency F_{LO}.

The following takes the experiment data of a preferred embodiment as an example to prove the effect of the present invention in real practice. The transmission frequency F_{tx} of the embodiment is 1725MHz. A local oscillating frequency F_{LO} synthesized by the frequency synthesizer 12 of the phase lock loop 30 is 1897.5MHz, and the reference signal S_{re} is generated by the first programmable divider 14. When the baseband signal for modulating the reference signal S_{re} has not been inputted, the output spectrum of the transmission frequency F_{tx} of the phase lock loop 30 is shown in FIG. 3. FIG. 3 is an experimental data curve of the transmission frequency as the first programmable divisor M of the phase lock loop 30, shown in FIG. 2, is equal to 11. The horizontal axis in FIG. 3 represents the frequency, and the vertical axis represents the power, wherein each unit in the horizontal axis means 300kHz. The maximum power of the transmission frequency F_{tx} is the predetermined transmission channel, meaning that the transmission frequency F_{tx} is 1725MHz. From FIG. 3, when the first programmable divisor M of the first programmable divider 14 of the phase lock loop 30 is equal to 11, the maximum output power of the transmission frequency F_{tx} is the apex A_1, 1725MHz. However, the spur frequencies A_2 and A_3, not equal to 1725MHz, also appear on the two sides of the frequency 1725MHz at 500 kHz. Because the reference frequency 26MHz used by the frequency synthesizer has the multiple frequency 1898MHz (26×73=1898), and the multiple frequency is very close to the local oscillating frequency 1897.5MHz, the interference occurs. After the interference passes the phase lock loop, the spur frequency A_2 and A_3 are generated on the two sides of the transmission frequency F_{tx} 1725MHz at about 500kHz.

Because the local oscillating signal corresponded to the transmission frequency

F_{tx} 1725MHz divided by the first programmable divisor 11 interferes the transmission frequency F_{tx}, the first programmable divider 14 further adjusts the first programmable divisor M to 9, and the corresponded local oscillating frequency is changed to 1940.625MHz. This frequency 1940.625MHz is far away from another multiple frequency 1950 MHz (26×75=1950). Referring to FIG. 4, FIG. 4 is an experimental data curve of the transmission frequency as the first programmable divisor M of the phase lock loop 30, shown in FIG.2, is equal to 9. From FIG. 4, when the first programmable divisor is adjusted to 9, the maximum output power B_1 of the transmission frequency F_{tx} is still 1725MHz, but no spur frequency appears on the two sides of the frequency 1725MHz any more.

A local oscillating frequency F_{LO} synthesized by the frequency synthesizer 12 of the phase lock loop 30 is 1897.5MHz, and the reference signal S_{re} is generated by the first programmable divider 14. The output spectrum of the transmission frequency F_{tx} of the phase lock loop 30, after the reference signal S_{re} is modulated by the inputted baseband signal, is shown in FIG. 5. FIG. 5 is an experimental data curve of the transmission frequency F_{tx} modulated by the baseband signal shown in FIG. 3. The horizontal axis in FIG. 5 represents the frequency, and the vertical axis represents power, wherein each unit on the horizontal axis means 300kHz. The maximum power of the transmission frequency F_{tx} is also the predetermined transmission channel, meaning that the transmission frequency F_{tx} is 1725MHz. As shown in FIG. 5, when the first programmable divisor is equal to 11, and after modulated by the baseband signal, the spur frequency C_2 and C_3 appear on the two sides of the main transmission frequency C_1 in the output spectrum of the transmission frequency F_{tx}.

Referring to FIG. 6, FIG. 6 is an experimental data curve of the transmission frequency modulated by the baseband signal shown in FIG. 4. When the first programmable divisor is adjusted to 9, there is no spur frequency on the output spectrum of the transmission frequency F_{tx}, except the main transmission frequency D_1. Therefore, the first programmable divider of the present invention can effectively solve the problem of the transmission frequency F_{tx} when the local oscillating

frequency is interfered by a specific multiple frequency and further eliminate the noise in the RF signal.

Referring to FIG. 7, FIG. 7 is a flow chart of the generating method of the RF signal of the phase lock loop 30 shown in FIG. 2. According to the present invention, the RF signal is generated where the phase lock loop 30 receives a baseband signal that has an input frequency Fi, and modulates the baseband signal to be a corresponding RF signal. The RF signal has a predetermined transmission frequency F_{tx} for transmitting. The method comprises the following steps:

S40: Start;

S42: Generating the local oscillating signal with the local oscillating frequency F_{LO} and dividing the frequency of the local oscillating signal by the first programmable divisor M to generate the reference signal S_{re};

S44: Modulating the reference signal S_{re} according to the baseband signal Fi to generate a corresponding first comparison signal S1, after the phase of the reference signal S_{re} is shifted by 90 degrees;

S46: Dividing the local oscillating frequency F_{LO} by the second programmable divisor N and generating the second comparison signal S_2 according to the difference between the feedback signal S_{FB} and the local oscillating frequency F_{LO};

S48: Detecting the phases of the first comparison signal S_1 and the second comparison signal S_2 to output a corresponding current-controlled I/O signal S_{IQ} corresponding to a phase shift of two signals;

S50: Receiving the current-controlled I/O signal S_{IQ} to generate a corresponding control current and filtering the control current I to output a control voltage V;

S52: Generating the corresponding RF signal to be transmitted according to the control voltage V, with the RF signal as a feedback signal S_{FB} by feeding back;

S54: End.

FIG. 8 is a function block diagram of a phase lock loop according to another preferred embodiment of the present invention. The embodiment 50 illustrated in FIG. 8 is similar to the embodiment 30 discussed in FIG. 2, but adds a first filter 36, a second filter 38, a third filter 40, and a fourth filter 42 in some specific places to perform signal filtration for better signal quality and for improving overall performance. For simplified illustration, the same element used in both of the FIG. 2 and FIG. 8 would have the same numerical reference, and would not be explained again to avoid redundancy. Before entering the frequency converter 26, the frequency-divided local oscillating signal from the second programmable divider 34 is first filtered by the filter 36. After leaving the frequency converter 26, the signal is also filtered by the filter 38 and then goes to the phase detector 18. Similarly, the signal from the first programmable divider 14 is filtered by the filter 40, and is then inputted to the phase shift generator 32. The modulated signal from the modulator 16 would also go to the filter 42 first, and then go on to the phase detector 18. It is to remind that filters 36, 38, 40, 42 are not necessary at all times, and are provided for better signal quality and overall performance. Persons skilled in the signal processing and filtration field know in what situation a filter should be employed and what kind of filters is to be utilized.

The present invention provides a phase lock loop for receiving a baseband signal that has an input frequency and modulating the baseband signal to be a corresponding RF signal. The RF signal has a predetermined transmission frequency for transmitting. The phase lock loop comprises a frequency synthesizer, a first programmable divider, a modulator, a voltage-controlled oscillator, and a frequency converter. The first programmable divisor of the first programmable divider is programmable-controlled so as to prevent the occurrence of a spur frequency, besides the predetermined transmission frequency, in the RF signal due to the interfered local oscillating signal. By using the present invention, all channels of the GSM system, can select suitable local oscillating frequency, without causing the problem of lower

output signal quality.

With the example and explanations above, the features and spirits of the invention will be hopefully well described. Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.